
DESIGN PROJECT 3

ELECENG 2E14 – Electronic Devices and Circuits I

Section C01

Viha Tripathi (tripav2)

400504615

Submitted: April 7, 2025

Course Instructors: Dr. Yaser M. Haddara.

The student is responsible for performing the required work in an honest manner, without plagiarism and cheating. Submitting this work with my name and student number is a statement and understanding that this work is my own and adheres to the Academic Integrity Policy of McMaster University.

Viha Tripathi

400504615

Circuit Schematic

The 12-transistor CMOS XOR gate circuit diagram depicts PMOS (M1–M4, M9, M11) pulling output Y high and NMOS (M5–M8, M10, M12) pulling it low.

The logic behavior is as follows:

- When $A \neq B$, the output $Y = 1$
- When $A = B$, the output $Y = 0$

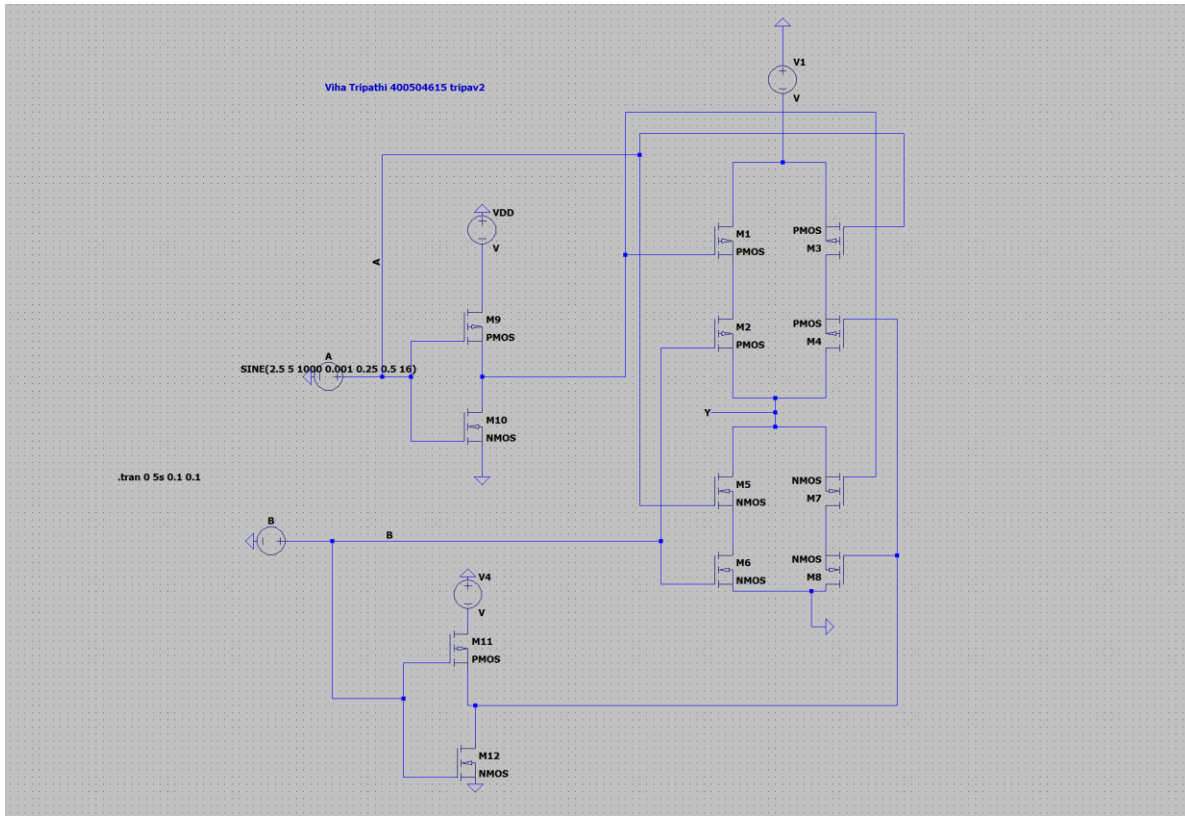


Figure 1: Circuit Schematic

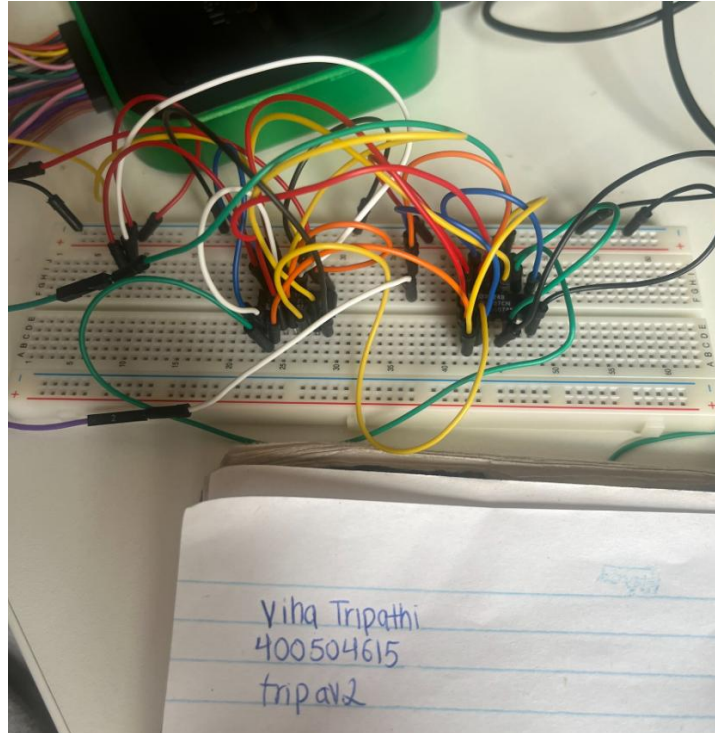


Figure 2: Physical Circuit

Ideal Sizing

In CMOS XOR gate design, transistor sizing is critical in realizing balanced and efficient switching. Since PMOS and NMOS transistors have different electrical characteristics, especially regarding carrier mobility, they must be sized to achieve symmetrical rise and fall times. In particular, electrons in NMOS transistors are more mobile than holes in PMOS devices; therefore, PMOS transistors need to be made wider to conduct a similar current. One popular ratio used in a 12-transistor XOR gate is 5:2, meaning that the PMOS devices are 2.5 times wider than the NMOS devices. This ratio in sizing also takes into account the internal gate structure of the XOR gate, where several transistors may be connected in series in the pull-up and pull-down paths. As the number of transistors in series increases, the effective drive strength reduces; therefore, a width increase is needed to maintain switching speed. The use of the 5:2 sizing ratio ensures that the gate maintains consistent performance, prevents skewed logic levels, and reduces delays caused by imbalanced charging and discharging of the output node. With this sizing technique, the gate can operate with better timing reliability under different loading conditions.

Hardware implementation

The 5:2 size ratio of PMOS to NMOS transistors would not be efficient to use in the hardware implementation because of constraints on the available individual components. All transistors used were the same size, thus all widths-to-lengths (W/L) for PMOS and NMOS devices were equal. This means that the circuit could not invoke the wider size of PMOS, which normally accounts for the lower mobility of holes. The consequence of this constraint is that transitions in the pull-up implementations are slower compared to those in the pull-down implementations, thus creating a mismatch in rise and fall times. In practice, this imbalance can cause signal degradation, a decrease in noise margin, as well as a small increase in propagation delay—an effect that is significantly noticeable during low-to-high output transitions. Despite the logical functionality being correct, performance is not as optimized as it could have been if with ideal sizing.

Functional Testing

The inputs were sequenced through all possible binary combinations on the digital I/O pins of the AD3 to test the XOR function. The output followed the XOR truth table, implying that the output will be high only when the two inputs are different. This is shown in both the timing diagram and the logic analyzer, where the output waveform matches exactly with the expected XOR function. Therefore, this proves that the circuit correctly performs the XOR function.

Table 1: DIO Pin Input Combinations and Corresponding XOR Output

DIO 0 (LSB)	DIO 1 (M)	DIO 2 (MSB)
0	0	0
0	1	1
1	0	1
1	1	0

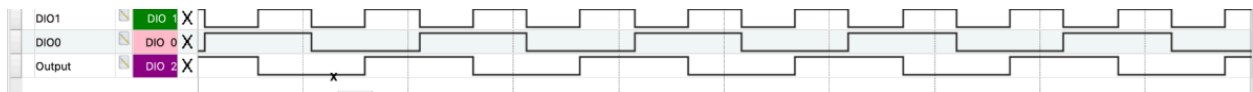


Figure 3: Logic Analyzer Waveform

Static Testing

One input was set to generate a 0V-5V square wave, while the other input was set to logic-1 (+5V). The output was then measured on an oscilloscope, enabling the measurement of the high (VH) as well as the low (VL) voltage levels. The original waveform output had readings ranging from 0.66V (VH) to 0.19V (VL). After reversing the two inputs, the second waveform gave

similar readings, with minimal difference in either VH or VL. This result supports the assertion that the output of the circuit does not depend on input order, as is expected with the XOR gate.

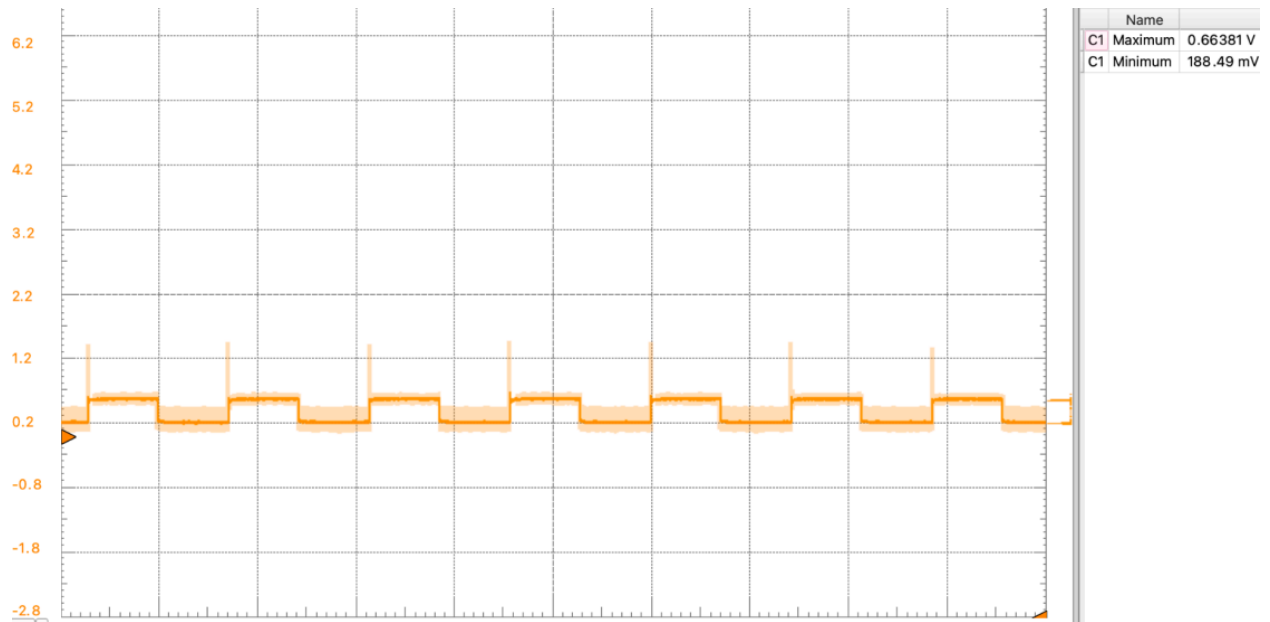


Figure 4: Static Level Testing Waveform (Input A = Square Wave, Input B = +5V)

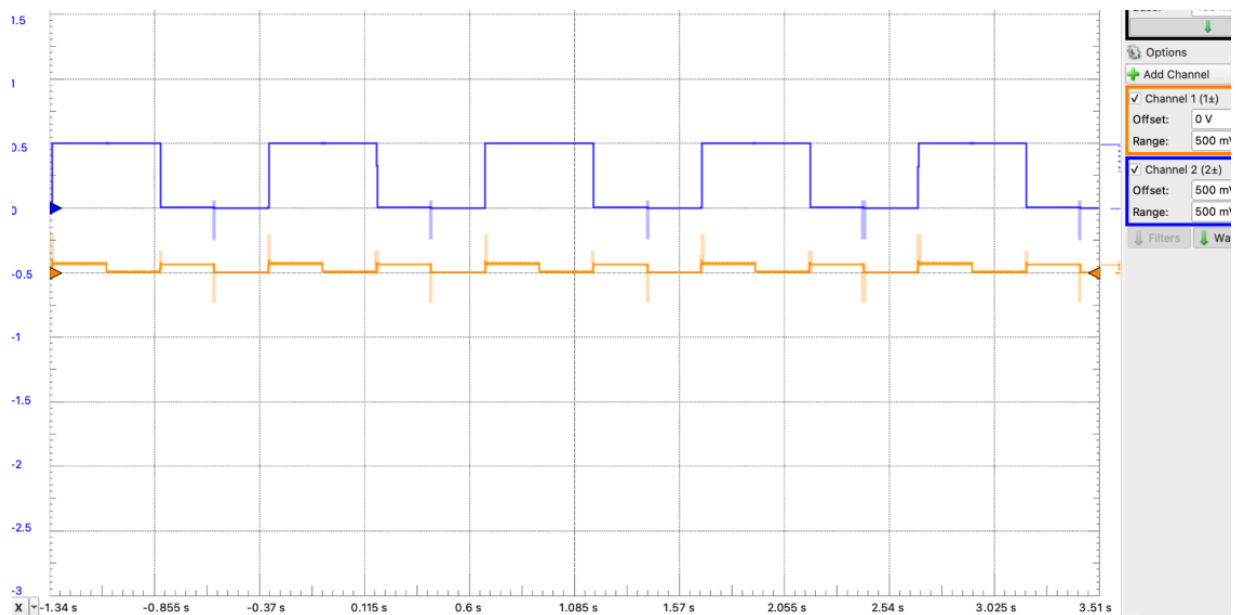


Figure 5: Static Level Testing (Input A = +5V, Input B = Square Wave)

Timing

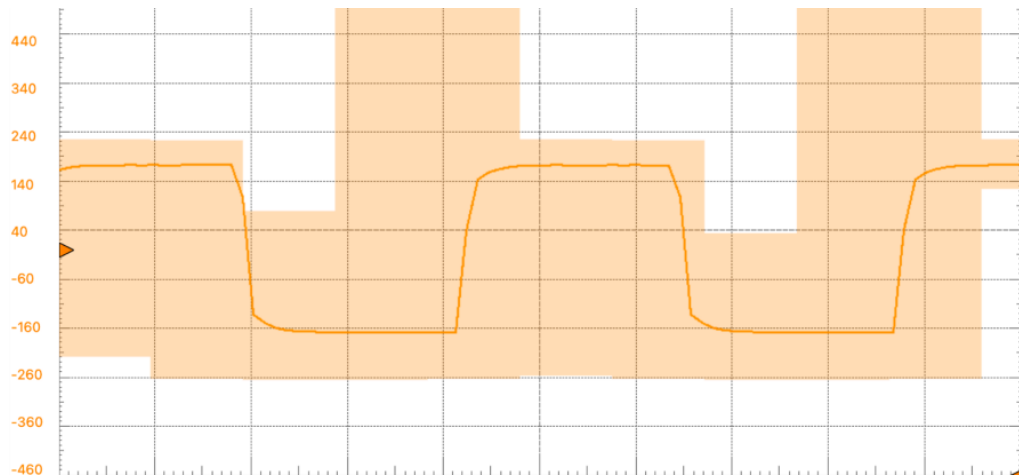


Figure 6: Timing Waveform

Rise and Fall Times:

Cursors were used on the oscilloscope to measure the time intervals between voltage thresholds during transitions. One input was held at the logic level of 1 (+5V) and the was driven by a square wave. The waveform measurements showed the rise time as the time taken by the output to go from about 10% to 90% of the high level as being around 50 μ s, and the fall time as the time taken to go from 90% to 10% as being about 32 μ s. These readings demonstrate how capacitive loading causes delays in the output, as well as show the transition behavior of the XOR gate in real loading conditions.

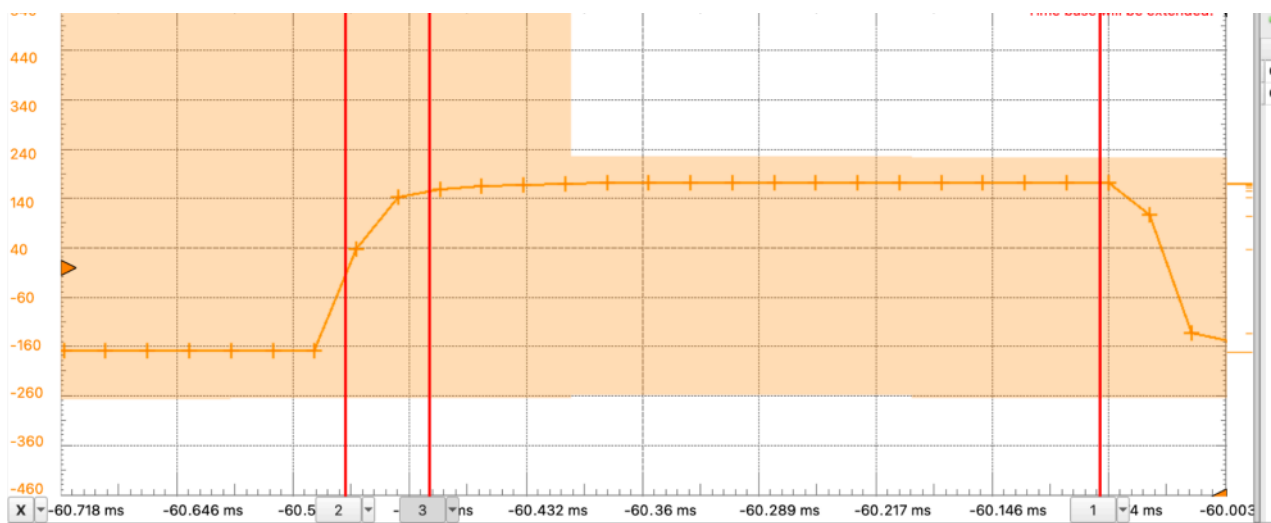


Figure 7: Rise Time



Figure 8: Fall Time

Propagation Delay

Two channels of the oscilloscope tool were utilized to measure the propagation delays, in particular tPLH (low-to-high propagation delay) and tPHL (high-to-low propagation delay). The input square waveform was captured on one trace, while the output of the XOR gate was observed on the other trace. The oscilloscope cursors were used to measure tPHL as the differential time from the output's falling edge to the input's rising edge, both measured at the 50% voltage level. This measurement gave a reading of the sensitivity of the gate to a rising input. A similar reading of tPLH was made from the input's falling edge to the output's rising edge, at the 50% crossing points. These measures give useful information regarding the XOR gate's transitions as well as the sensitivity of the XOR gate to capacitive loading. From the waveform measures, tPLH was 100.25 μs , and tPHL was 40.5 μs , making t_p 70.38 μs . These readings are useful in considering timing parameters in digital circuits, especially in those situations where signal speed and dependability are key considerations.

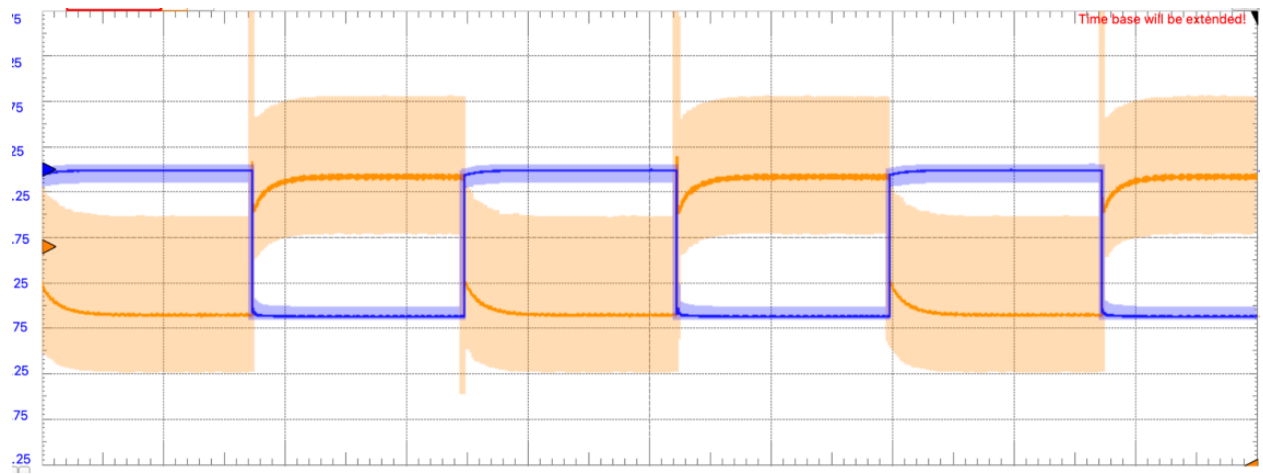


Figure 9: Propagation Delay Measurement